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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,030	01/28/2004	Richard K. Williams	M7207US4D	4737

27906 7590 05/03/2005

PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER	
KESHAVAN, BELUR V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,030	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Belur V. Keshavan	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11 and 16-19* is/are allowed.

6)☒ Claim(s) *2,5-10 and 12* is/are rejected.

7)☐ Claim(s) *3,4 and 13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2, 8, 10 and 12, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo (U.S. Patent No. 6,583,010) in view of Duffy et al. (3,655,457)

Regarding claim 2, Mo discloses a method of fabricating a MOSFET (40), in columns 3-5 and in figures 4 and 5, comprising: forming a trench (46) in a surface of a semiconductor (42), the trench defining a mesa (58); forming a first insulating layer (48) along a wall of the trench; forming a gate (50) in the trench by introducing polysilicon (52) into the trench, the gate being insulated from the semiconductor by the insulating layer (48); performing a plurality of implantations of dopant of a first conductivity type (58 and 66) into the mesa to form a body region wherein each of the implantations has a different energy (column 5, lines 19-45, and steps 514 and 516 in figure 5); and implanting dopant of a second conductivity type into the mesa to form source region (60). Thus Mo teaches all the features and limitations of claim 2 but lacks a dose that is the same as the dose for another of the implantations. However, the step of implanting the same dose with different energies into a body region to achieve an uniform doping is very well known in the art ~~of which the examiner takes an Official Notice~~. In support of this assertion, the examiner cites Duffy et al. wherein plurality of implantations are carried out with the same dose at different energies (column 7, lines 30-40 and figure 3D) to obtain an uniform doping in a semiconductor body. It would have been obvious to one of the ordinary skill in the art to use the teachings of Duffy et al. to modify or add to the method described in MO to achieve an uniform doping in the mesa to form a body region.

O.C.
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Regarding claims 8 and 10, Mo discloses, in column 4 lines 57-65 and figures 4 and 5, wherein forming the trench comprises: forming a hard mask on the semiconductor (step 506 in figure 5); and etching the semiconductor through an opening in the hard mask to form the trench (46) and forming a gate (50) in the trench by introducing polysilicon (52) into the trench.

Regarding claim 12, Mo discloses, in column 3 lines 53-54 and in figure 4, forming a second insulating layer (56) over the mesa; a contact opening in the second insulating layer and depositing a metal layer (72) into the contact opening to form an electrical contact with the source region (70). Mo is silent about etching the contact opening in the insulating layer. However the art of etching a contact opening through an insulating layer for electrical connection is ~~notoriously very well~~ known in the art~~, of which the examiner takes Official Notice~~. In support of this assertion, the examiner cites a textbook by Sze (Semiconductor Devices, Physics and technology, 1985, pp (451-452). Therefore it would have been obvious to a person of ordinary skill in the art to use the teachings Sze to modify or add to the method described by Mo to make electrical contact to the mesa.

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Claims 9, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mo.

Regarding claim 9, Mo discloses a method of fabricating a MOSFET (40), in columns 3-5 and in figures 4 and 5, comprising: forming a trench (46) in a surface of a semiconductor (42), the trench defining a mesa (58), wherein forming the trench comprises forming a hard mask on the semiconductor (step 506 in figure 5); and etching the semiconductor through an opening in the hard mask to form the trench (46); forming a first insulating layer (48) along a wall of the trench; forming a gate (50) in the trench by introducing polysilicon (52) into the trench, the gate being insulated from the semiconductor by the insulating layer (48); performing a plurality of implantations of dopant of a first conductivity type (58 and 66) into the mesa to form a body region wherein each of the implantations has a different energy (column 5, lines 19-45, and steps 514 and 516 in figure 5); and implanting dopant of a second conductivity type into the mesa to form source region (60). Mo specifically silent about a maximum implant energy for the implantations causing dopant of the first conductivity type to penetrate through hard mask into the semiconductor to a depth desired for a junction between the body region and a drain region. However, Mo teaches in column 7 and lines 39-42, about choice of implant energy and dose to achieve the desired physical and electrical characteristics of a semiconductor device. It is therefore obvious for a person of ordinary skill in the art at the time the invention was made to use the teachings of Mo to use a maximum implant energy for the implantations to cause dopant of the

first conductivity type to penetrate through hard mask into the semiconductor to a depth desired for a junction between the body region and a drain region to achieve the required electrical and physical characteristics of the semiconductor device.

Regarding claim 5, Mo discloses wherein a first of the implantations is at a first dose (column 5 line 21) and a second of the implantations is at a second dose (column 5 line 33), the second dose differing from the first dose.

Regarding claim 7, Mo discloses in column 5 lines 50-59, completing the MOSFET without performing a process to diffuse the dopant of the first conductivity in the body region, and in column 5 lines 19-25 wherein energies of the implantations control a depth of a body-drain junction at an interface between the body region and an underlying portion of the semiconductor.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mo in view of Sze (Semiconductor Devices, Physics and technology, 1985, pp (420).

Mo teaches all of the features and limitations of the base claim 9 but lacks chained implantations such that implantations in combination provide a uniform doping for the body region. However, the ~~chained~~ claimed implant technique is ~~notoriously~~ well known in the art ~~of which the examiner takes Official Notice~~. In support of this assertion, the examiner cites Sze wherein the combination of implantations is used to achieve an uniform doping for the body region. It would have been obvious to one of ordinary skill in the art to the use the teachings of Sze to modify or add to

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the method described in MO with the objective to minimize the vulnerability of the device to punch through breakdown.

Allowable Subject Matter

Claims 3, 4, 13, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11,16, 17, 18 and 19 are allowed

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V. Keshavan whose telephone number is 571-272-1894. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BVK.
04/25/05.

OLIK CHAUDHURI
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